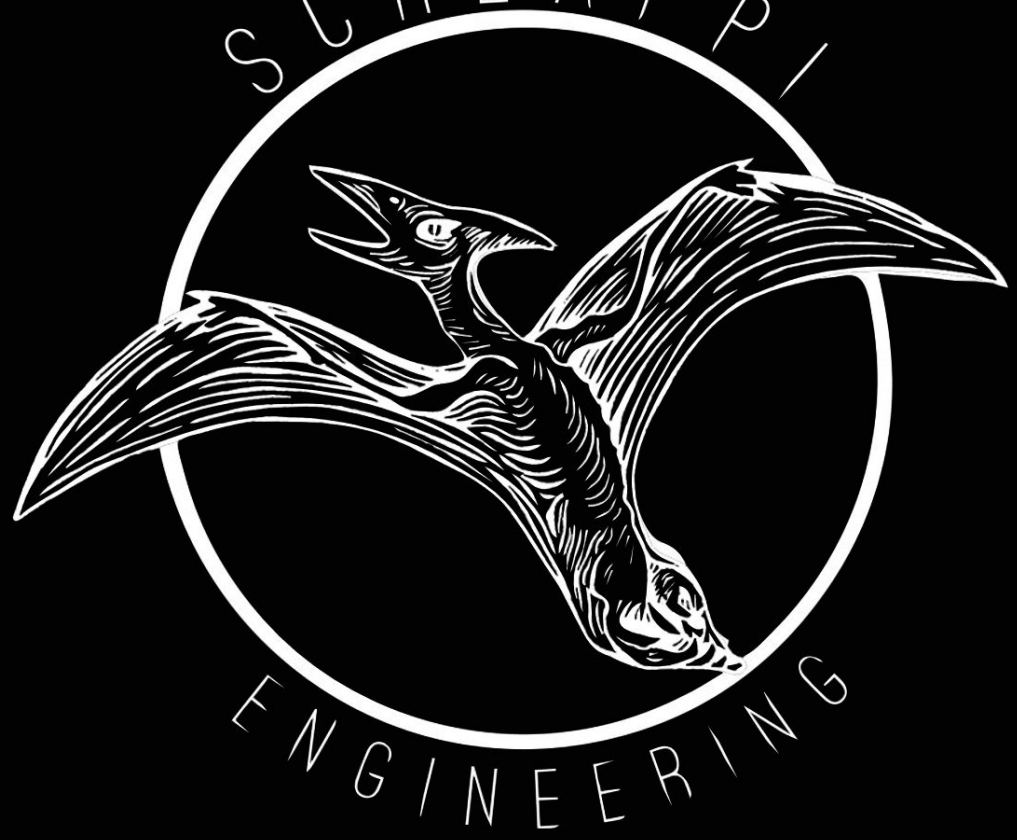


Post-Synthesis: Adventures in using FPGAs for Eurorack Synthesizer Modules

What is the Three Body

- A triple digital oscillator with an analog interface
- A digital platform with two PCBs
  - FPGA board with Lattice ECP5 with 12k LUTS
  - Control board with inputs and outputs
- Design goals
  - Analog style interface
  - Digital features
  - High quality audio rate cross modulation
    - High internal sample rate
  - Learning FPGA workflow with a “simple”project

Workflow

- What I used
  - Toolchain
    - Verilog
    - Yosys/Nextpnr
    - A text editor
    - Verilator and GTKwave for simulation
  - Hardware
    - Lattice ECP5 FPGA

OSS CAD Suite

linux-x64 passing | darwin-x64 passing | windows-x64 passing

linux-arm64 passing | darwin-arm64 passing

Introduction

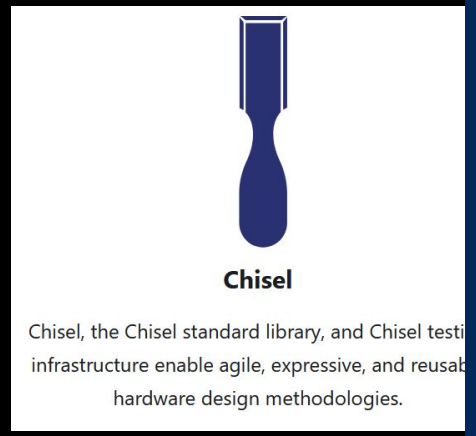
OSS CAD Suite is a binary software distribution for a number of open source software used in digital logic design. You will find tools for RTL synthesis, formal hardware verification, place & route, FPGA programming, and testing with support for HDLs like Verilog, Migen, and Amaranth.

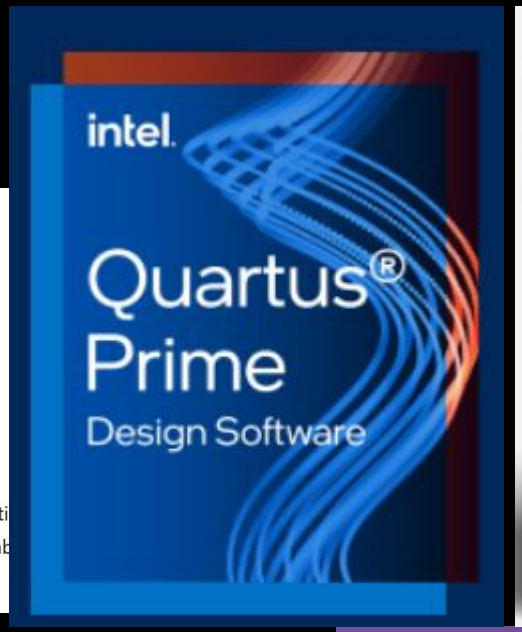
OSS CAD Suite is a component of YosysHQ's Tabby CAD Suite:

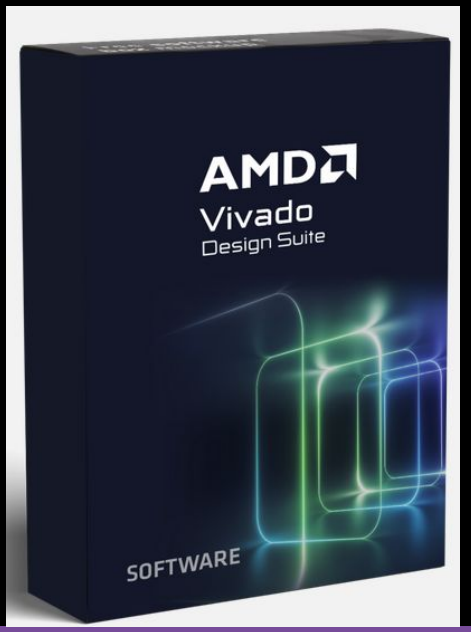
See Tabby CAD Datasheet for details on Tabby CAD Suite; see OSS CAD Suite GitHub (this page) for details on OSS CAD Suite.

Workflow

- What I did not use (but may or may not have made my life easier)
  - Vendor tools
    - Traditionally bloated and unwieldy
    - Many come with useful building block IP
  - A modern HDL or SOC builder
    - Amaranth
    - Chisel
    - Litex
  - A coprocessor of some sort

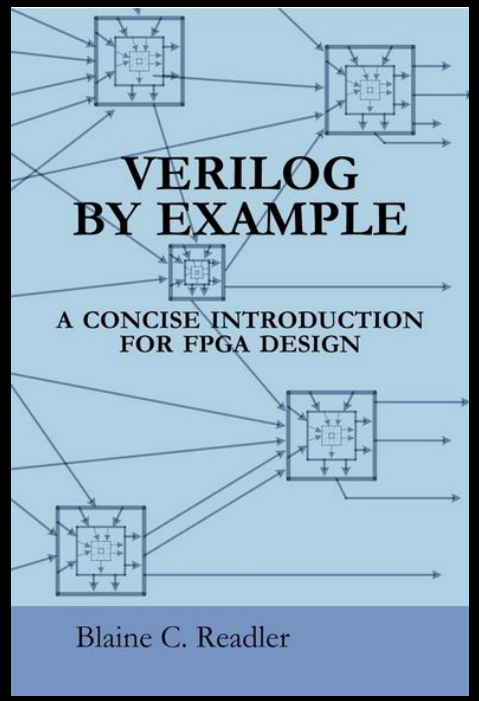


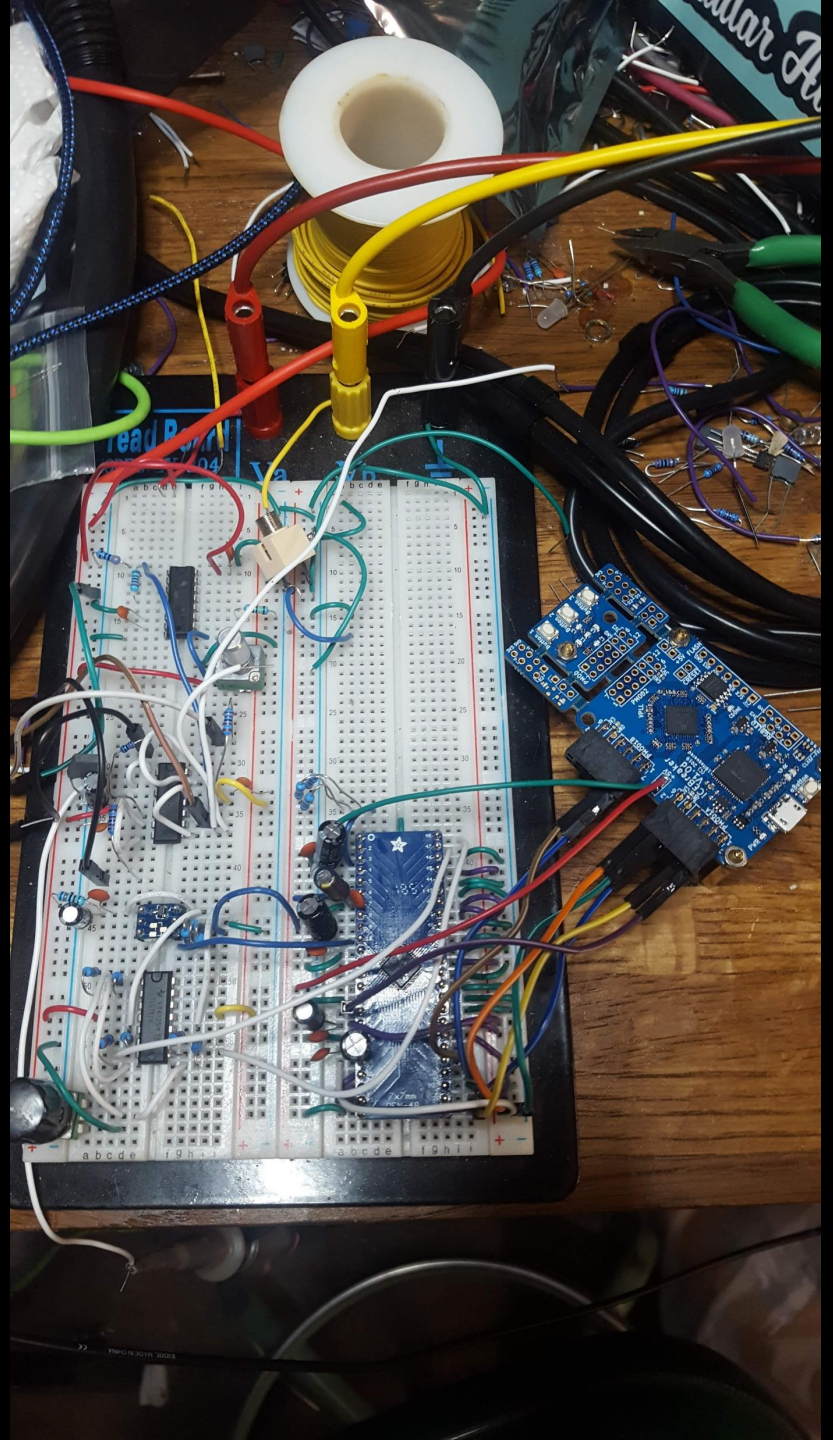




How it started (Fall 2019)

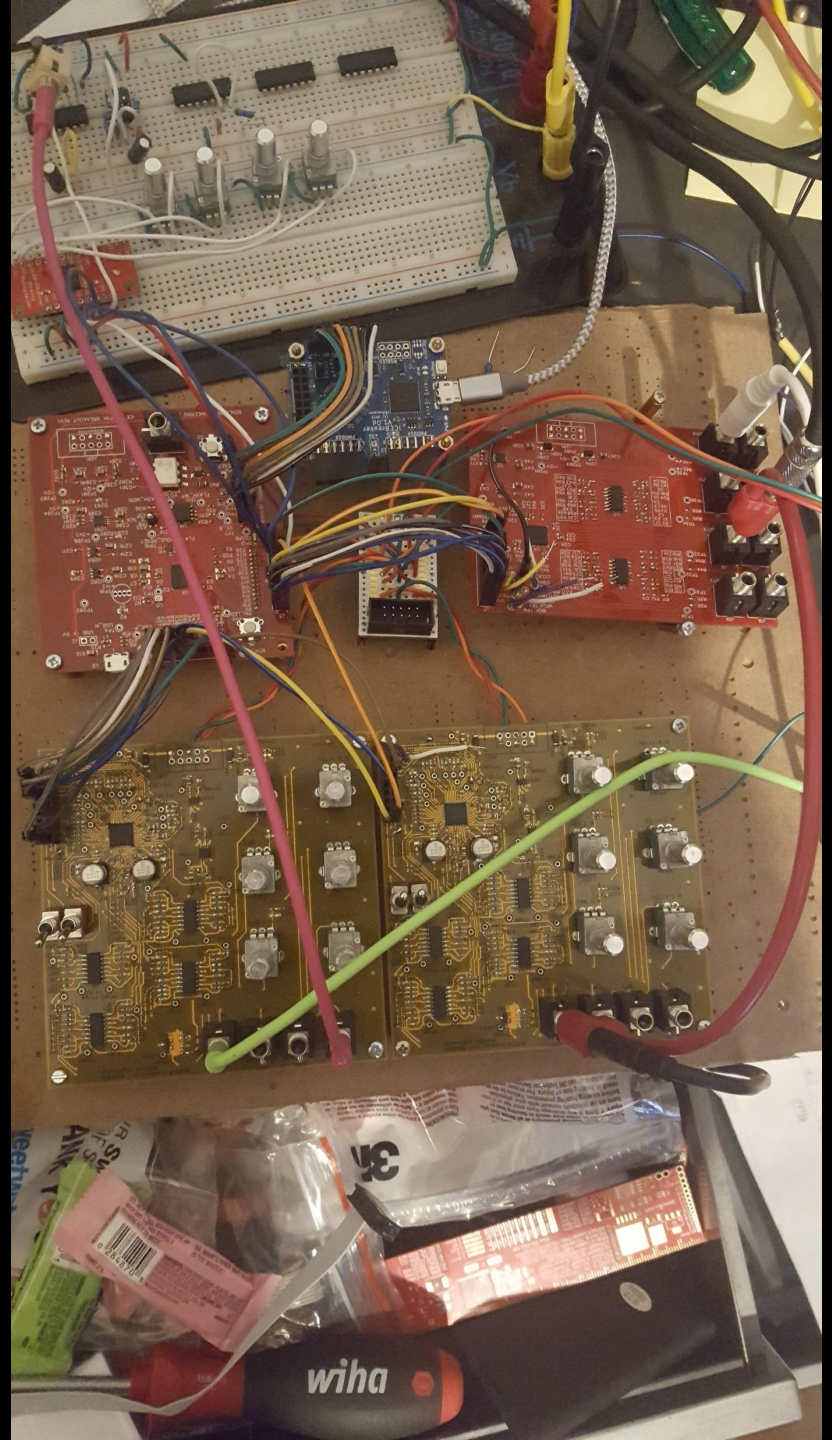
- Icebreaker dev board and a breadboard
- In my garage learning Verilog
- Lots of gotchas in the open source toolchain
  - Compiling the toolchain took forever
  - Basics like how to set up the PLL hard to figure out
  - (most of these things have been fixed)





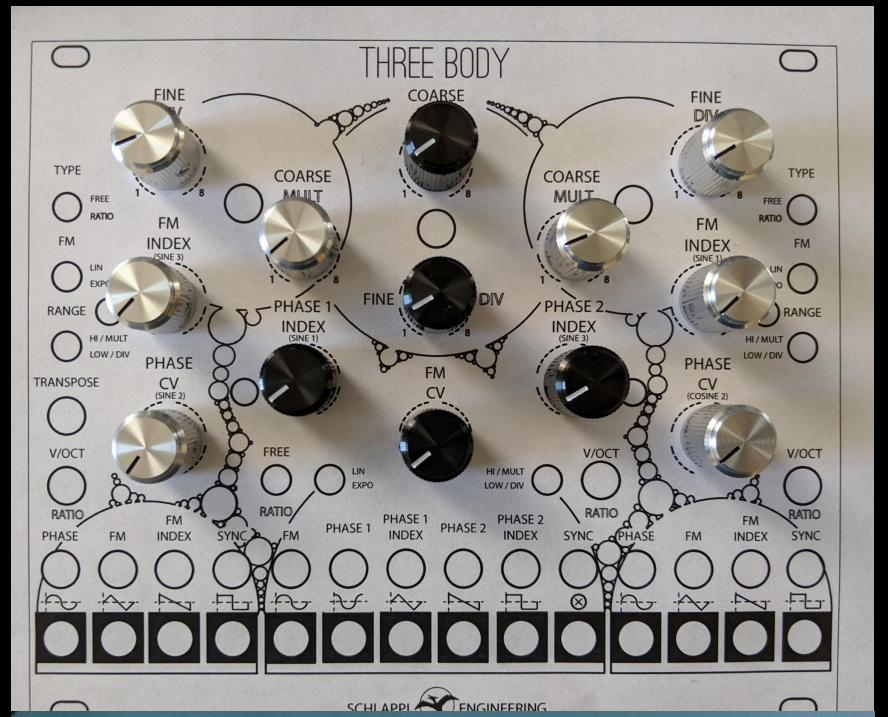
First iterations (Winter 2019)

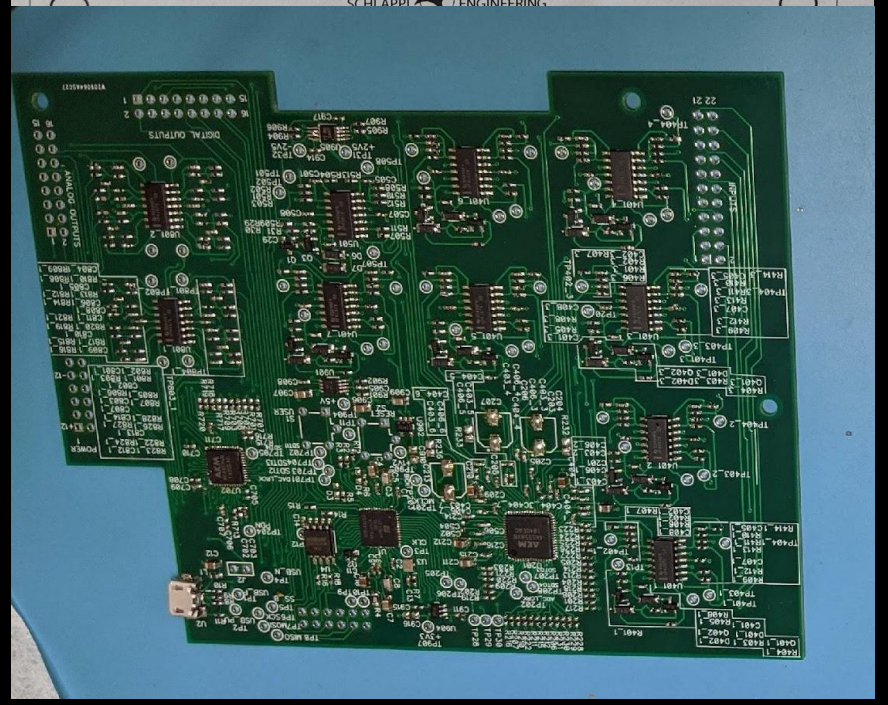
- Icebreaker dev board
- Custom ADC and DAC breakout boards
  - Using octal AKM I2s audio converters
  - Mounted on packing material



Rev 1 (Winter/Spring 2020)

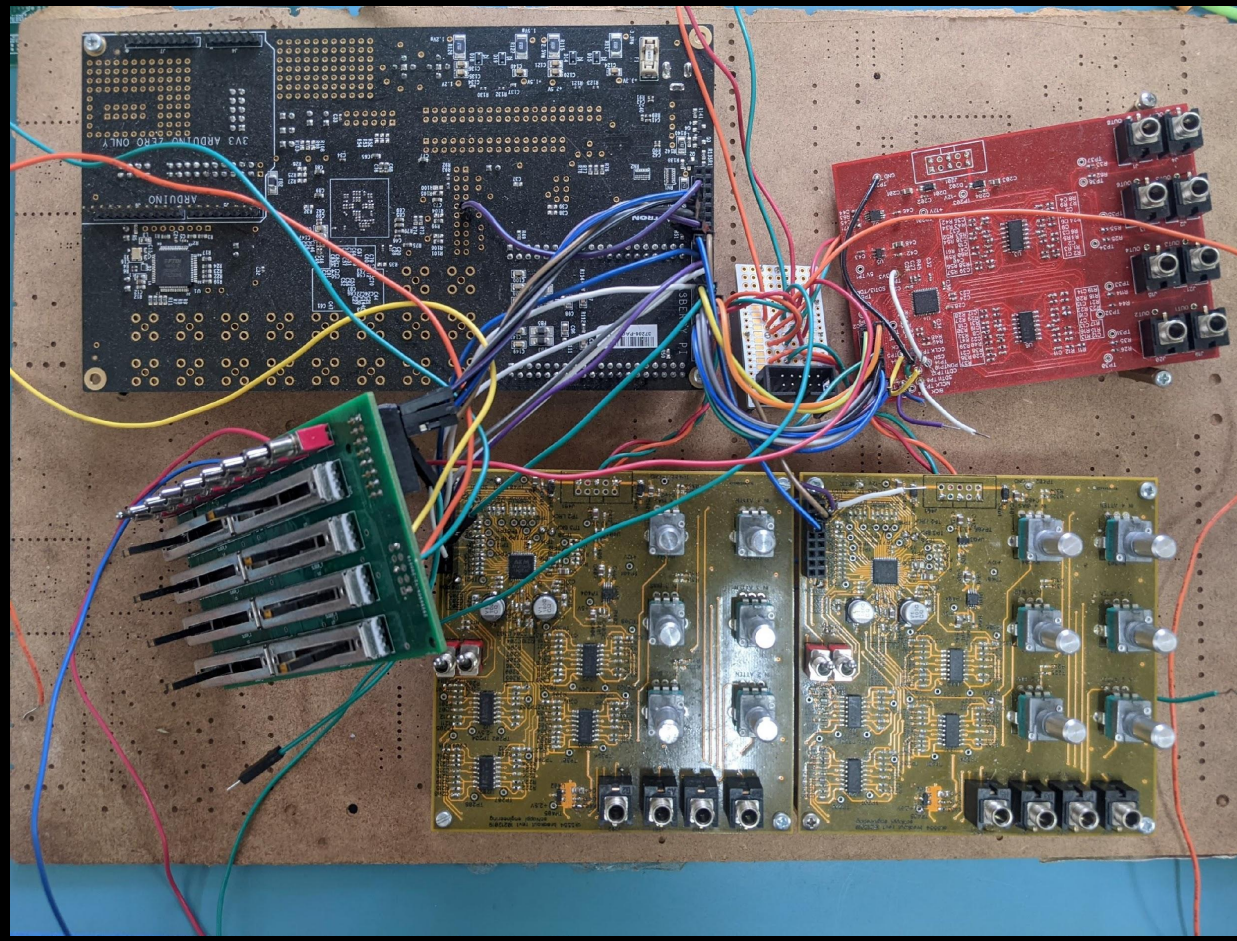
- Interface design
- Two 4 layer boards
  - Interface board with analog vcas for indexes
  - Digital board with converters and ice40
- Issues
  - The UP5K only has eight 16 x 16 multipliers (DSP slices)
  - It can be difficult to meet timing (25Mhz) with a complex design
  - I spent a lot of time prematurely optimizing the design to get it to work on the ICE40 then having to undo and redo that work as I added or changed features
  - The I2S ADCs are not intended for DC signals and very heavy filtering was required to get decent performance from the ADCs





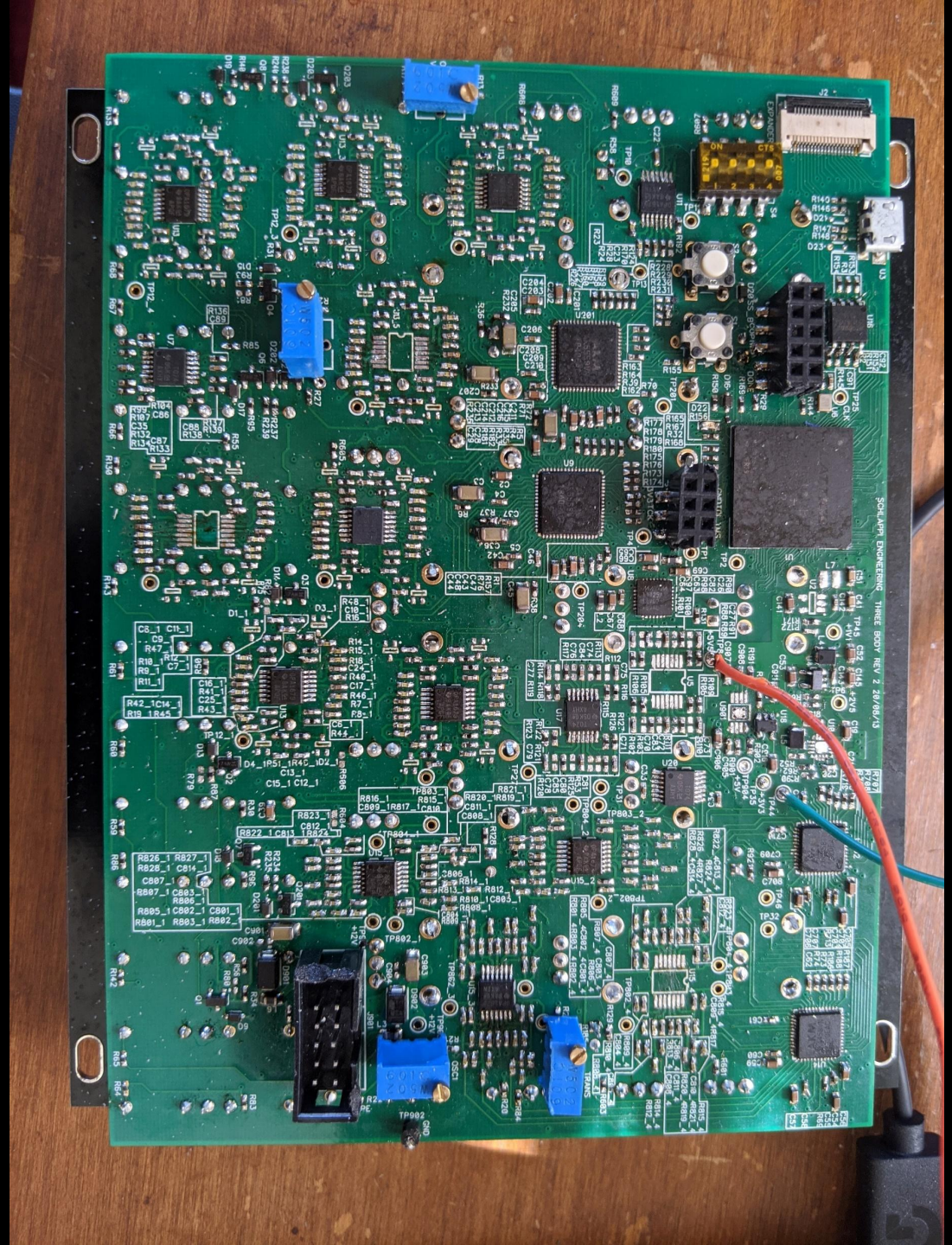
Back to the dev board (Winter/Spring 2020)

- Put the Lattice versa in place of the Ice40 to try the ECP5
  - Thanks Jared!
- Undid most of my optimisations (much simpler logic)
- rewrote the Three Body to take advantage of:
  - Faster fpga fabric (50MHz master clock)
  - More and larger multipliers (28, 18x18)
  - More block RAM (32 blocks)



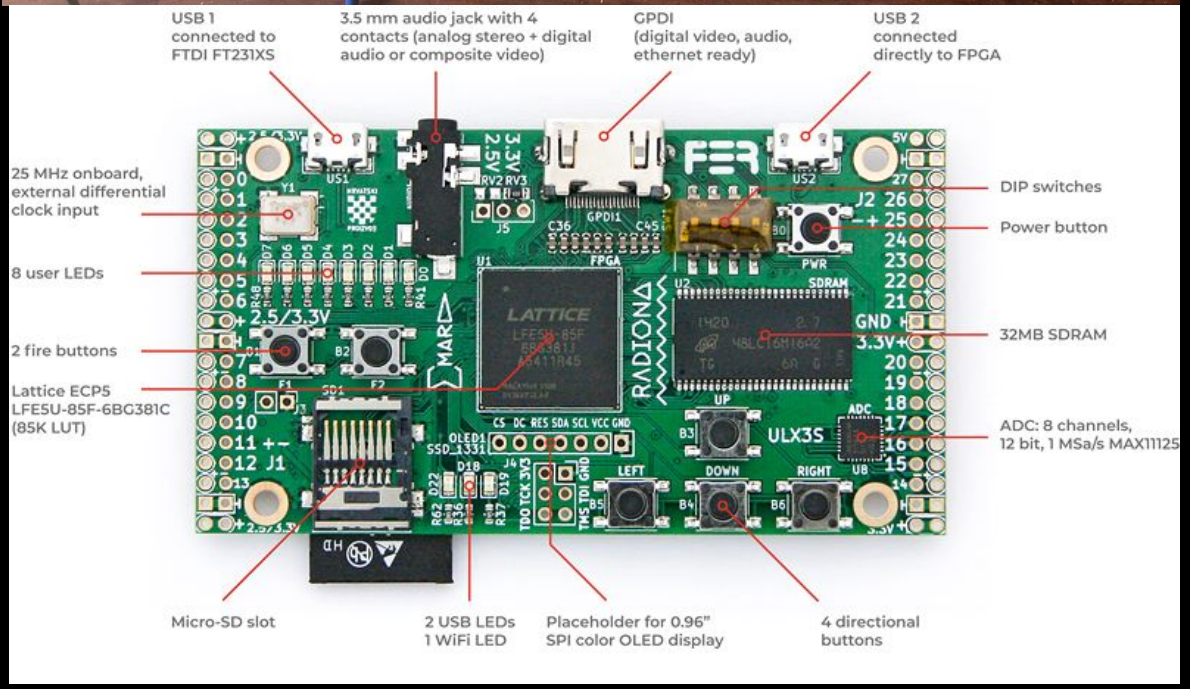
Rev 2
(Fall/Winter 2020)

- Single 6 layer board with ECP5 12k
  - Total nightmare to debug
  - AKM factory burnt down
  - Never got it to work
  - Total depression



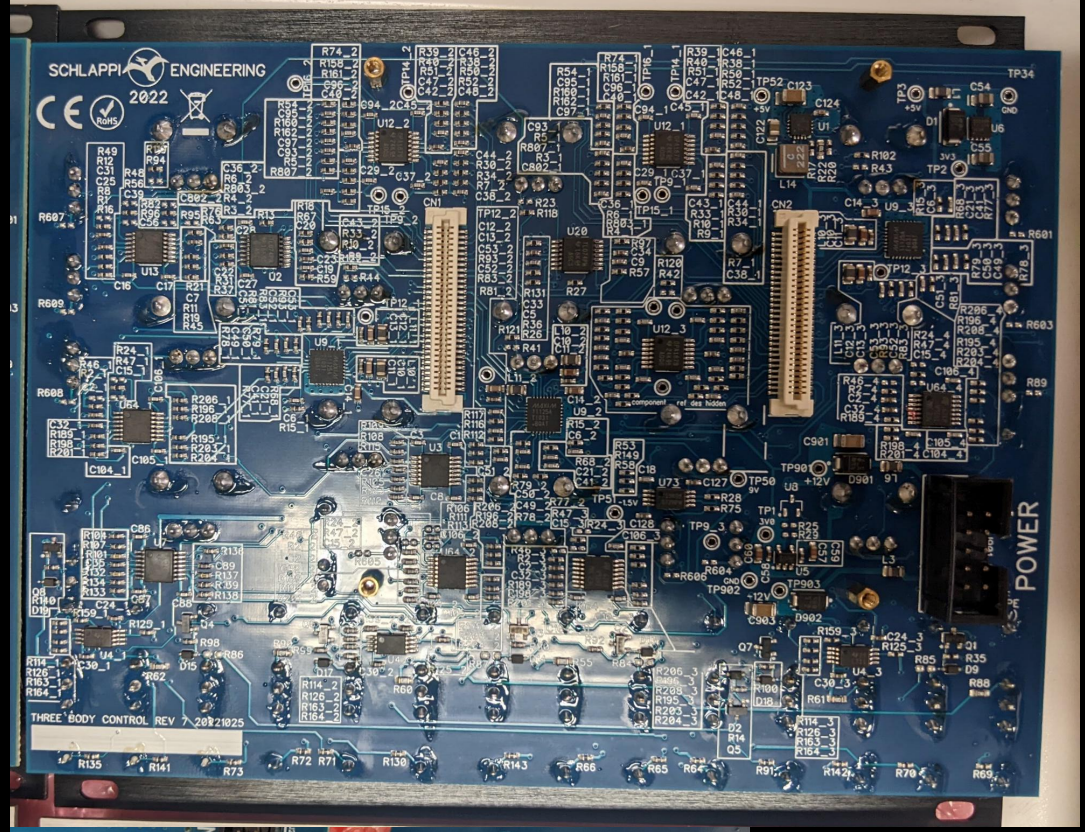
Detour and recovery from failure (Fall 2021)

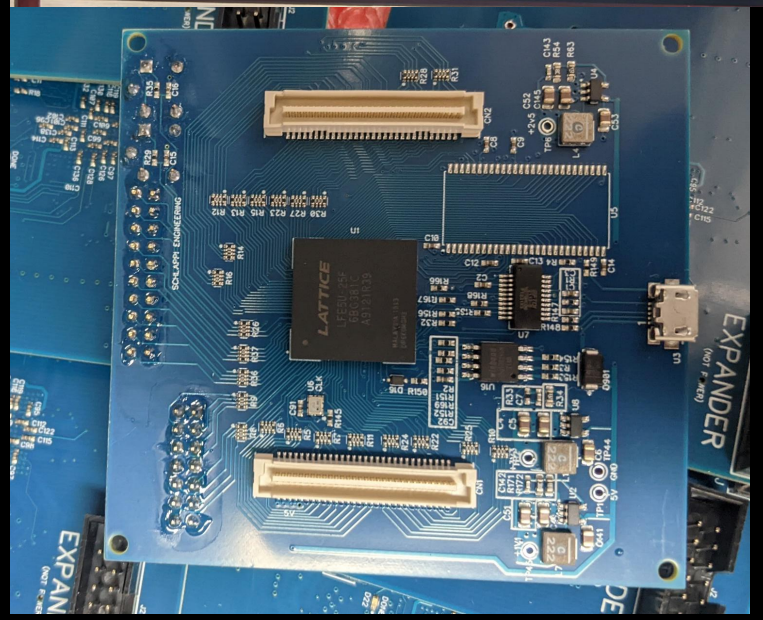
- Made a big weird thing with forty sliders on it to try out ideas and clear my head
  - (also released another module, Boundary)
- Radiona ULX3s dev board
- Maxim industrial 12 bit SPI SAR ADCs (same as on ULX3S)
- 2nd order 16 bit delta sigma DACs in the FPGA fabric using an open source Verilog core and differential analog filters based on the data sheets from commercial designs



Current Design
Rev 3-6
Released October 2022

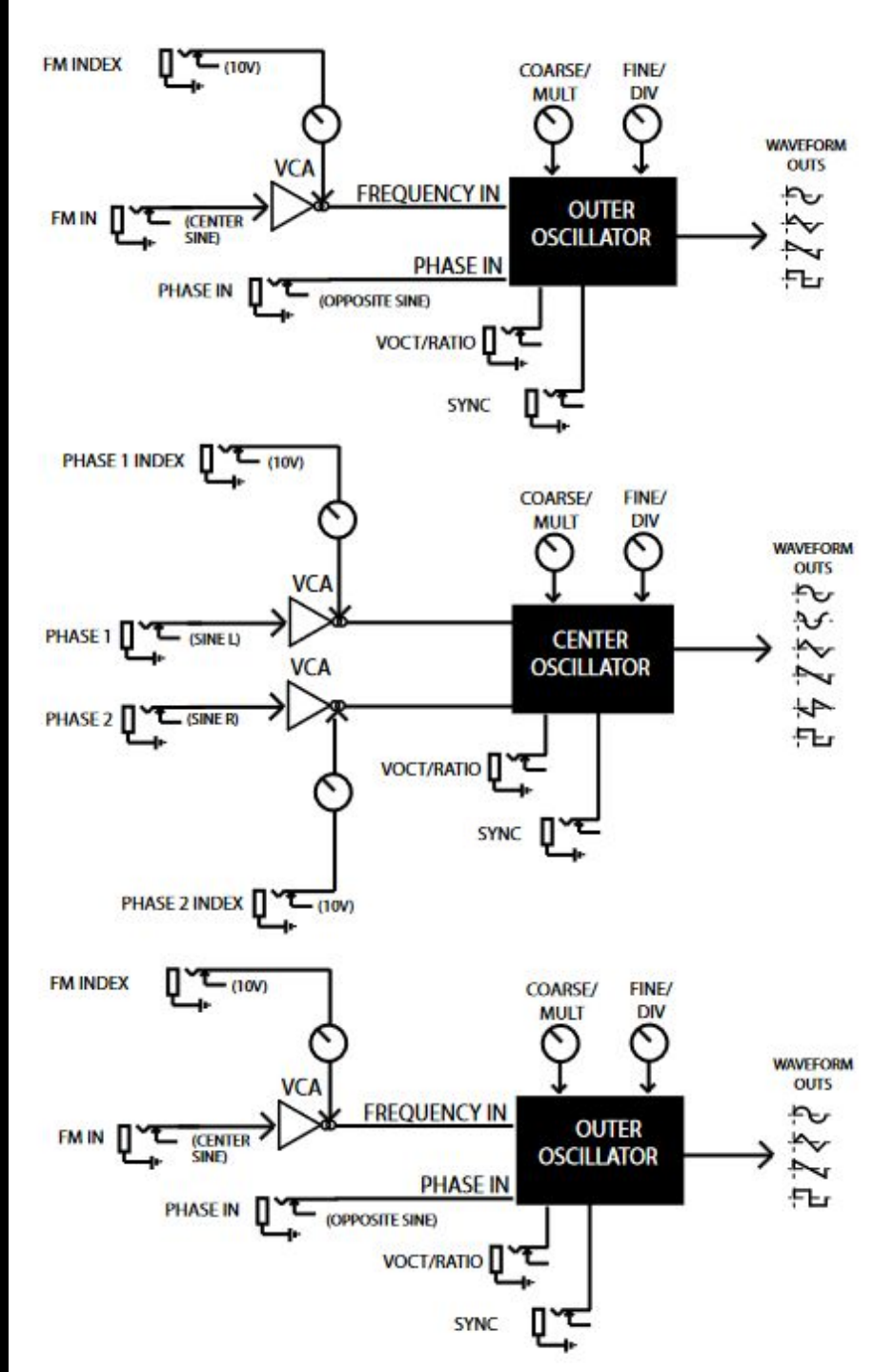
- Went back to a two board layout
- Brain board (4 layers)
  - ECP5, Flash, FTDI usb, SDRAM (not used)
- Control Board (4 layers)
  - Max11125 12 bit ADCs
  - Filters for differential 2nd order delta sigma DAC in fpga fabric
  - Voltage regulators and references





Hardware Capabilities

- 24 channels of simultaneous ADC running at 12 bit 96kHz
  - 6 of these channels are devoted to panel potentiometers
    - There is no particular need for these to be running that fast
    - No reason not to run them that fast
  - 4 volts per octave inputs
  - 11 modulation inputs
  - 3 channels set aside for calibration etc
- 4 logic inputs
  - Comparator inputs used for sync



Hardware Capabilities

- 11 channels of DAC running at 16 bit 96 (ish) kHz
  - I used an open source second order delta sigma DAC written in Verilog and ran it at 25MHz
    - It takes up very little space on the fpga
  - I implemented a differential reconstruction filter with nice op amps based on data sheets from commercial delta sigma DACs
  - Tested gives very solid 16 bit performance with relatively low distortion
- There are three square wave outputs driven directly from a pin to avoid slewed edges or aliasing of a DAC
- This allows me to make a design which very closely mimics the feel and feature set of an analog oscillator

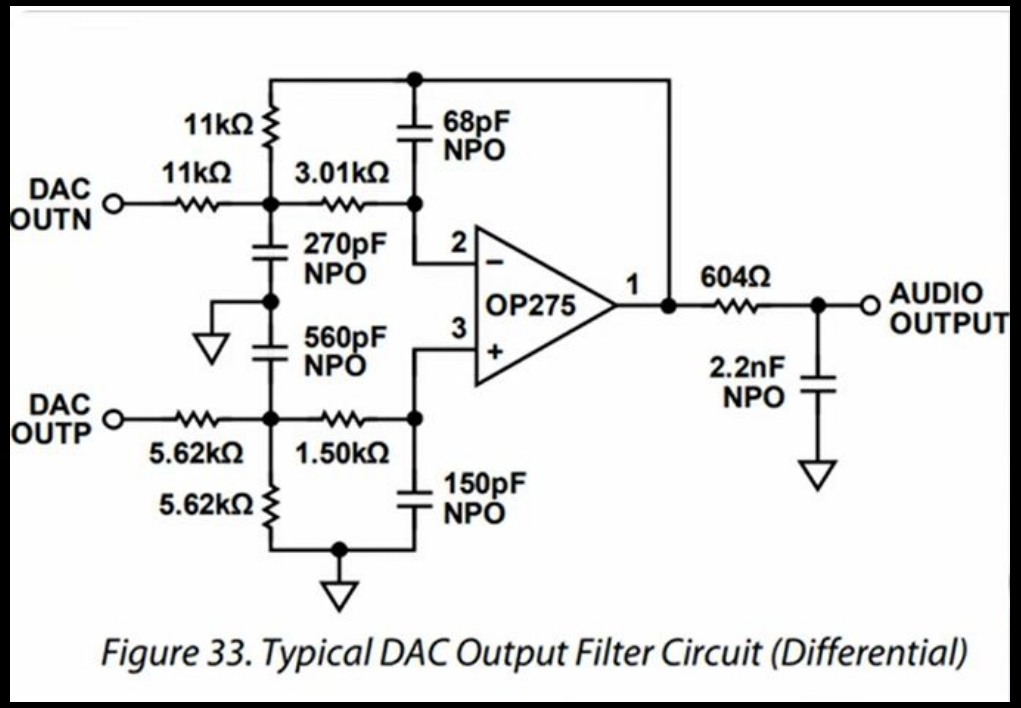
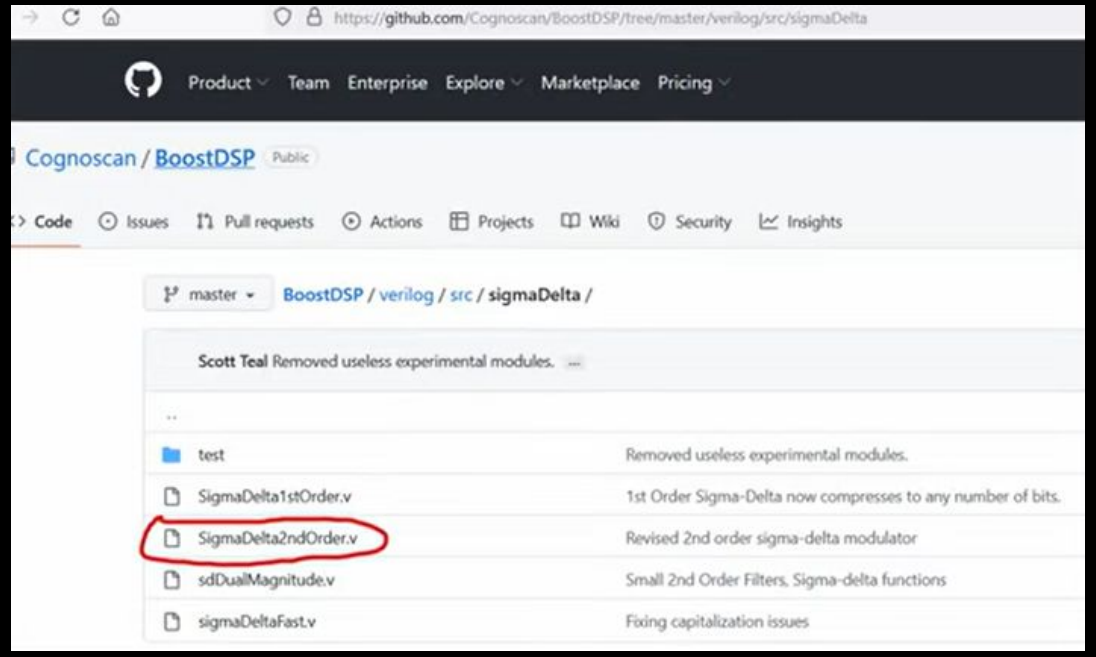
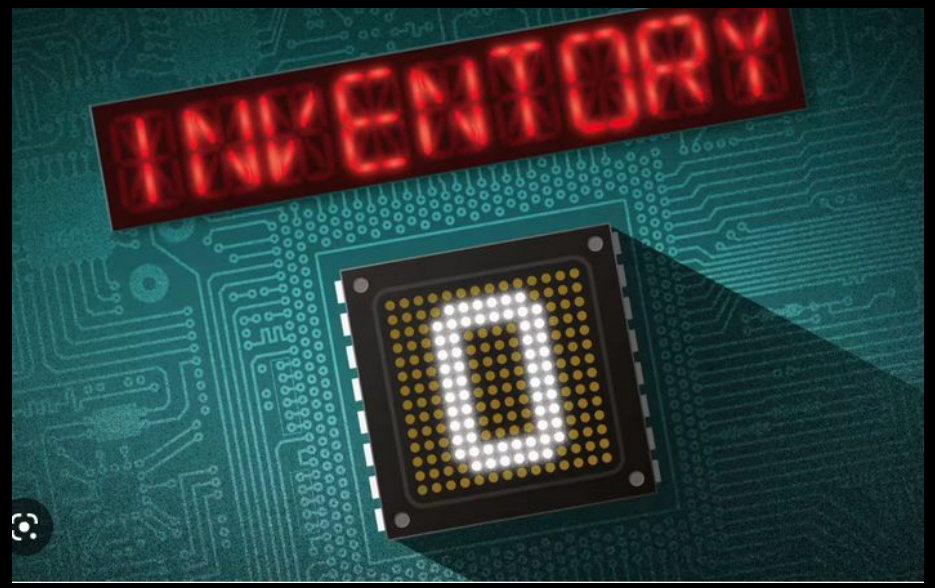


Figure 33. Typical DAC Output Filter Circuit (Differential)

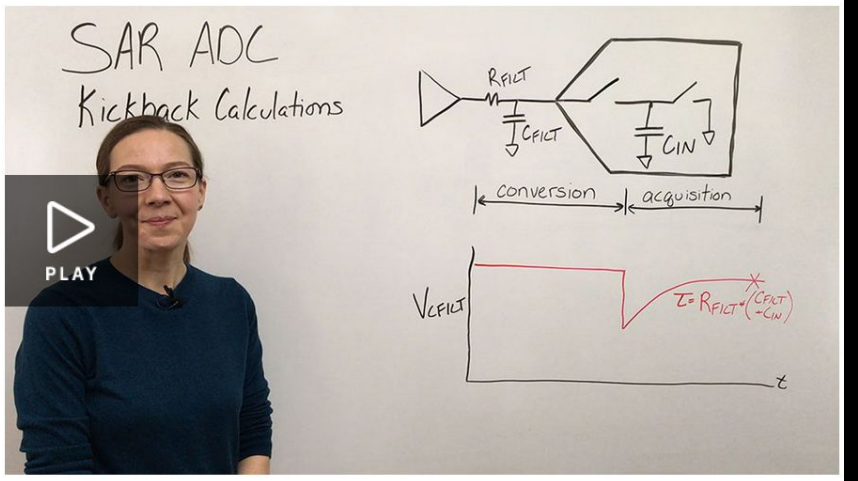


- Difficulties and lessons learned:
  - I spent a lot of time trying to figure out a soft core to use in calibration routines and to talk to the SPI flash memory
    - Ended up doing it in logic, winbond has a a simulation of the memory you can download and use in the open source ecosystem
  - Multiplexed ADCs require fairly fast op amps to charge the internal capacitor and you also need to be careful that they can drive this capacitance and stay linear
  - Attention has to be paid to make sure the correct voltage reference is selected to get temperature compensation in line with the accuracy you are looking for
  - Find parts during the IC shortage was extremely painful. FPGAs, appropriate op amps, voltage references, and voltage regulators were all issues



Driving SAR ADCs Part 2: Kickback Calculations

WATCH SERIES



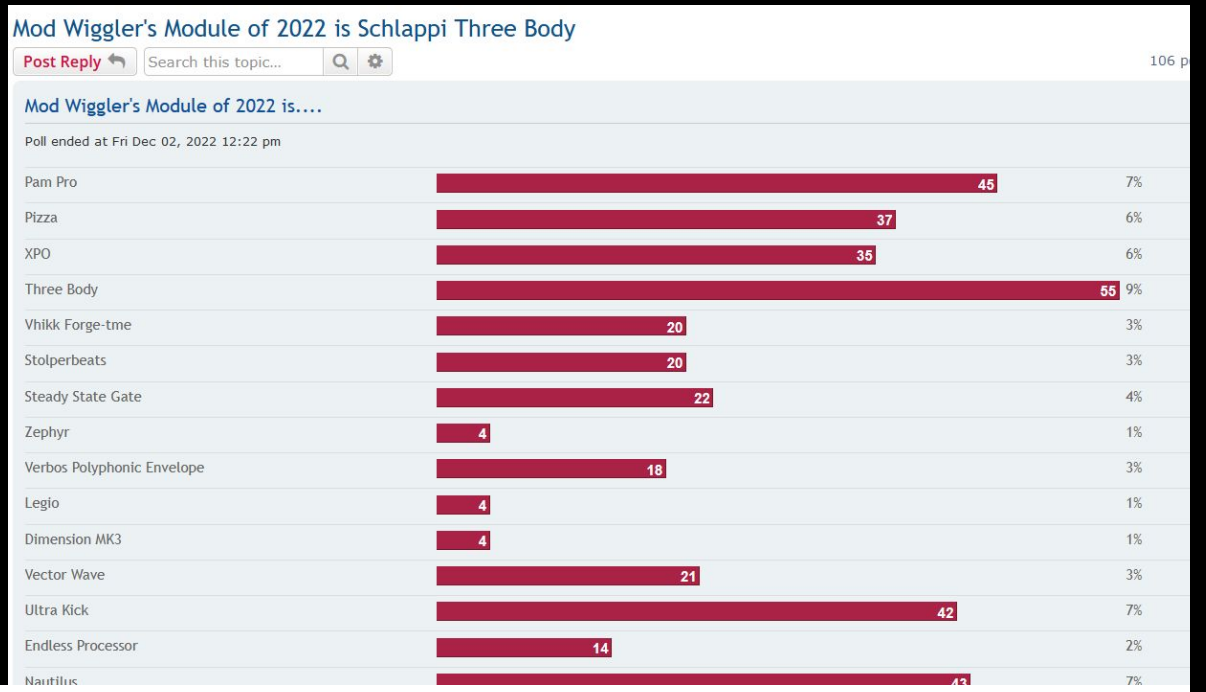
Review formulas for SAR ADC kickback amplitude and time constant.

Voltage Reference Recommendation for Data Converters

VOLTAGE REFERENCE	ADC RESOLUTION (1)	DAC RESOLUTION (1)
TL431LI, TLV431	10-b	8-b
LM4040, LM4050, REF30	12-b	10-b
REF31, REF33, REF4132	14-b to 16-b	12-b
REF34, REF50	16-b to 18-b	14-b to 16-b
REF70	18-b+	16-b+

End result

- The project took around three years to complete
  - But now I feel reasonably competent in Verilog and digital hardware design
- The first run of 250 sold within a month (October 2022)
- Second run of 300 became available in March 2023
- The Three Body has been well received
- More FPGA projects to come (eventually)

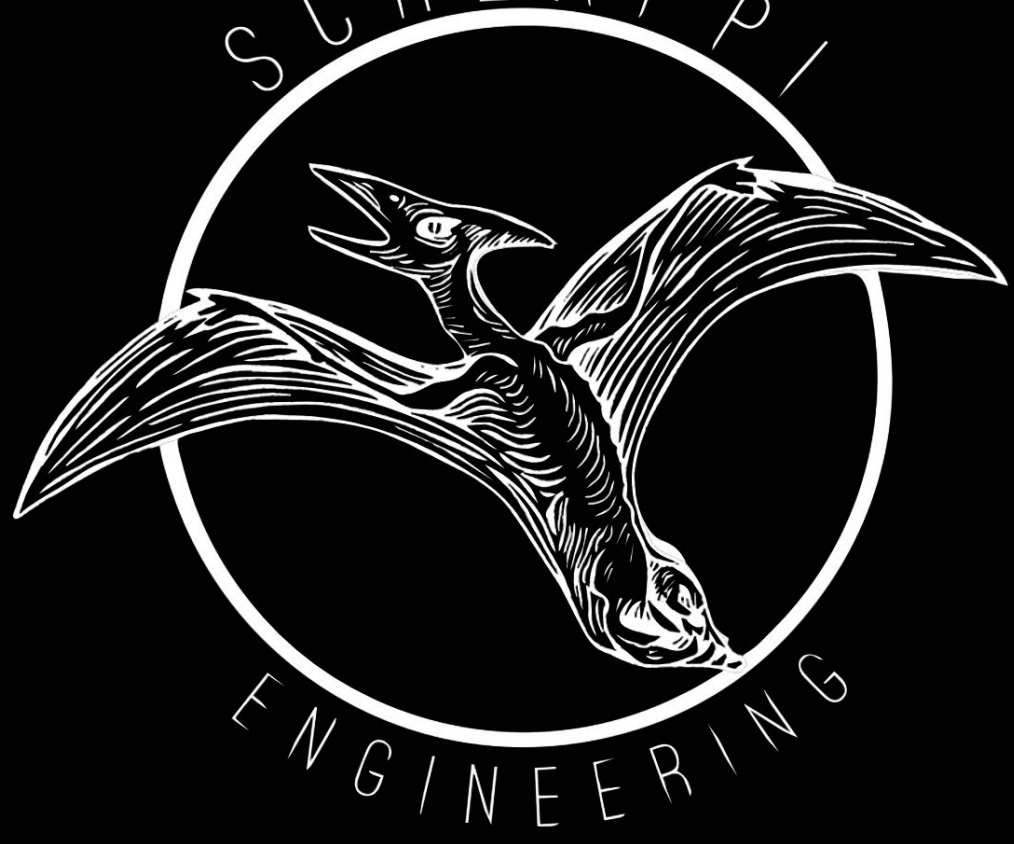


What have I been doing since the Three Body

- Exploring the musicality of basic digital structures in four bit cmos logic implementations
  - Accumulators - Nibbler (Released Jan 2024)
  - Logic functions - BTMX (Releasing June 2024)
  - ADC/DAC - BTFLD (available soon, August 2024?)
- Designed several more analog modules (unreleased)
- Why?
  - Not everything needs an FPGA (or MCU)
  - It was hard to buy them for a while
  - Fundamental structures are interesting to me

What FPGA related prototyping have I been doing since the Three Body

- I designed a bunch of different peripheral boards and connected them to my fpgas
  - AKM Audio ADCS (you can buy them again)
  - 12 bit ADCS
  - Video ADC and DAC
  - Various control boards
- I spent a long time working on time based processing (delays and related effects) on an ECP5 using SDRAM and the open source toolchain and got really frustrated with the available ram controller
- I got annoyed at how much more expensive the Lattice chips are now than they were before the Chip shorted
- I bought a bunch of different dev boards and tried out some toolchains outside the open source toolchain
  - Efinix
  - Gowin



Thanks for listening!